REMARKS

Claims 1-15 remain pending in this application. Claims 1, 3, 6, and 12 are independent. Claims 1-4, 6-10, and 12-15 have been amended, and no claims have been added or canceled by this amendment.

Objection to the Claims

Withdrawal of the objection to claims 1, 2, 6, and 12-14 is requested. These claims have been amended in a manner that is believed to overcome the stated bases for objection.

Indefiniteness Rejection Under §112¶2

Withdrawal of the rejection of claims 2, 4, 6, 8-10 under 35 U.S.C. §112, second paragraph, as being indefinite, is requested. These claims have been amended in a manner that is believed to overcome the stated bases for indefiniteness.

Anticipation Rejection By Joshi et al.

Withdrawal of the rejection of claims 1-8 and 10-14 under 35 U.S.C. §102(b) as being anticipated by Joshi et al (US Patent 5,954,815) is requested.

Applicant notes that anticipation requires the disclosure, in a prior art reference, of each and every limitation as set forth in the claims.[1] There must be no difference between the claimed invention and reference disclosure for an anticipation rejection under 35 U.S.C. §102.[2] To properly anticipate a claim, the reference must teach every element of the claim.[3] "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference".[4] "The identical invention must be shown in

[1] *Titanium Metals Corp. v. Banner*, 227 USPQ 773 (Fed. Cir. 1985).
[2] *Scripps Clinic and Research Foundation v. Genentech, Inc.*, 18 USPQ2d 1001 (Fed. Cir. 1991).
[3] *See* MPEP § 2131.
[4] *Verdegaal Bros. v. Union Oil Co. of Calif.*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

as complete detail as is contained in the ...claim."[5] In determining anticipation, no claim limitation may be ignored.[6] The applied art fails to meet this threshold requirement, at least with respect to the independent claims, as amended.

Discussion of Joshi et al. and Distinctions

Joshi et al. is directed to a computing system that invalidates instructions in fetched instruction blocks upon predicted two-step branch operations with second operation relative target addressing. Only a portion of Joshi's invention shown in Figure 3 deals with a function that is somewhat similar to Applicants' disclosed and claimed invention.

Joshi et al. discloses an instruction queue (50) that holds excess instructions that cannot be bypassed directly to the registers below (22a-22d). Once the queue has instruction in it, the registers are fed from the queue instead of the bypass.

Joshi et al. bypasses the instruction queue when the registers are empty, and load into both the registers and the queue at the same time. However, they only load into the queue those instructions that will not fit in the registers.

In contrast, Applicants' disclosed and claimed invention simultaneously loads the same instructions into both the decoder stage and the instruction queue when they are empty or contain invalid data. Thereafter, each stage (decode & IQ) process the instructions independently. The decode stage performs branch prediction, and IQ performs dispatch. Then, any branch predict taken information from decode feeds into the IQ stage to invalidate instructions.

Specific Deficiencies of Joshi et al.

The applied art does not disclose a method for decreasing the latency between an instruction cache and a pipeline processor having a plurality of parallel execution stages, each

[5] *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).
[6] *Pac-Tex, Inc. v. Amerace Corp.*, 14 USPQ2d 187 (Fed. Cir. 1990).

execution stage having a decode stage and an instruction queue for sequentially processing instructions being processed by the processor, wherein the method includes, among other features, "…simultaneously inserting instructions from said instruction cache in parallel to said decode stage and instruction queue when said decode stage and said instruction queue contain invalid data", as recited in independent claim 1, as amended.

Further, the applied art does not disclose a method for processing instructions in a pipelined processor having a series of pipelined stages which reduces latency between an instruction queue and a pipeline processor, wherein the method includes, among other features, "…simultaneously loading one or more of said fetched plurality of instructions into said instruction queue and into said decoder when said instruction queue and decoder are both empty; sequentially loading each of said fetched instructions into said instruction queue from said decoder when said instruction queue and said decoder are not empty…", as recited in independent claim 3, as amended.

In addition, the applied art does not disclose a method for executing instructions in a pipelined processor, wherein the method includes, among other features, "…determining if said fetched instructions are stored in a cache memory; determining whether both a decode stage of a decoder and an instruction queue stage of an instruction queue of said pipelined processor are empty; [and] simultaneously loading said fetched instructions from said cache memory into said decode stage and into said instruction queue stage in parallel when both said decode stage and said instruction queue stage are empty…", as recited in independent claim 6, as amended.

Finally, the applied art does not disclose a apparatus for reducing the latency between stages of a pipelined processor, wherein the apparatus includes, among other features, "…a multiplexer associated with said one of the plurality of locations, wherein, depending on a value of the valid bit, said multiplexer supplies said one of the plurality of locations in the instruction queue with either an output of one of the decode stages or an output of the instruction cache, [and] wherein, when the output of the instruction cache is supplied to said one of the plurality of

locations in the instruction queue, the output of the instruction cache is simultaneously supplied to said one of the decode stages", as recited in independent claim 12, as amended.

Accordingly, since the applied art does not disclose all the claimed limitations of independent claims 1, 3, 6, and 12 as amended, reconsideration and allowance of claims 1-15 are respectfully requested.

Unpatentability Rejection over Joshi et al. in View of "FOLDOC"

Withdrawal of the rejection of claim 9 under 35 U.S.C. §103(a) as being unpatentable over Joshi et al. (5,954,815) in view of the "Free On-Line Dictionary of Computer" ("FOLDOC") is requested.

At the outset, Applicant notes that, to establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, ***the prior art reference must teach or suggest all the claim limitations***.[7] Further, the teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure.[8]

Whether or not FOLDOC teaches that for which the Examiner offers it, FOLDOC does not make up for the previously identified deficiencies of Joshi et al., as discussed above with respect to independent clam 6, from which claim 9 depends.

Accordingly, since the applied art does not disclose all the claimed limitations of claim 9, reconsideration and allowance of this claim are respectfully requested.

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[7] *See* MPEP §2143 (***emphasis*** added). .
[8] *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991) and *See* MPEP §2143.

Conclusion

In view of the above amendment and remarks, Applicants believe that each of pending claims 1-15 in this application is in immediate condition for allowance. An early indication of the same would be appreciated.

In the event the Examiner believes an interview might serve to advance the prosecution of this application in any way, the undersigned attorney is available at the telephone number indicated below.

Although no fees are believed to be due with this response, for any fees that are due, including fees for extensions of time, the Director is hereby authorized to charge any fees or credit any overpayment during the pendency of this application to CBLH Deposit Account No. 22-0185, under Order No. 20421-00072-US from which the undersigned is authorized to draw.

Dated: January 4, 2006

Respectfully submitted,

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